

Abstract. Verification of software and technical systems has always been and still remains one of the most significant tasks since appearance of first computing devices. Today there are quite a lot of approaches to solve this problem. However, development of such formal verification method as Model Checking helped to solve the problem of verifying systems representation and to unify verification process for software and technical systems. Its main idea is to transform an original system into a unified form. It means that a verification process requires only a model that would most precisely describe system's behavior.

The article considers the possibility of system model construction using RLTL-notations (Recursive Linear Temporal Logic), which are a recursive representation of formulas of linear temporal logic. However, its usage is not limited to this aspect. The advantage of using RLTL for these purposes is that models based on it might be verified in respect to requirements which are also RLTL-based without casting to any another data structure. It will certainly help to simplify and improve the performance of a verification process. Furthermore, the article describes the formal tools, which allow simplifying RLTL-based models in many cases reducing the number of their states and transitions.

Keywords: verification, Model Checking, RLTL equation characteristics, Kripke structure, Buchi automaton, temporal logic formula, LTL, CTL.

References

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Примеры библиографического описания статьи

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